

DC6688SLP-USB Rev3.2 User Manual

User Manual of DC6688SLP-USB Rev3.2 Single Line Programmer for DC6688F family with USB interface

User Manual Document Revision 1.8

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1 Introduction

This document briefly describes the details of the programming tool "Single Line Programmer for DC6688F family with USB interface" with model number "DC6688SLP-USB Rev3.2".

1.1 Ordering Information

Device Name	Single Line Programmer for DC6688F family with USB interface
Model Number	DC6688SLP-USB

1.2 Features

- Standalone download data to devices without connection to PC
- ♦ 1 to 10 download data to up to 10 devices simultaneously
- Optimized Speed download 2KB data to flash in 1.6 seconds
- ♦ 2-color LED indicate downloading result
- ♦ Backlight LCD show device and customer information
- ♦ SLP Software simple user interface

1.3 Package

- 1. Single Line Programmer (SLP)
- 2. Power Adaptor with 5VDC/1A Output
- 3. USB2.0 Cable
- 4. User Manual

1.4 Useful Links

- 1. SLP Page download latest software installer and user manual http://www.dragonchip.com/TechDoc/DevelopmentTools/SLP.htm
- 2. Technical Website of DC6688 Product Family http://www.dragonchip.com/TechDoc/DC6688.htm
- 3. Technical Website of DC6388 Product Family http://www.dragonchip.com/TechDoc/DC6388.htm

2 Hardware



Side View



3 SLP Software

Install the SLP software (Rev8.0.4 or above) by the software installation CD.

3.1 Minimum System Requirements

- Microsoft Windows 7/8/10
- > Intel Pentium 4 CPU running at 1.5GHz or higher

3.2 User Interface

	SLP C	Options
Operating Mode/	🔇 SLP.exe [Software Development]	X
Export/Import	M Operating Mode → 👜 Export → 🖄 Import → 🚯 Help → 🌄 About	DragonFLASH™
Select Device	Family DC6688 Product DC6688FST Part No. DC66	88F30ST/STT/STE
and SLP Board revision	SLP Board Clock Frequency Op DC66688SLP-USB Rev3.1 12.000 MHz N	otion o. of Ports Enable 1 💌
	Firmware	Buzzer 🔽
	Program Flash Size (KB) -Please Select-	Download to IC 🕅
	Program File D:DC6688\Demo-IC.hex Browse	rmware ID
Select path of	Fill Unused Byte: O 0x00 O 0xFF 🗖 Read Lock	Model: Ver. :(PF)CS
Firmware files	Data File [D:DC6688\Data.bm	0123:4567:A31B
	Custom Info DADC6688VCI.bin Transformed Lock	ownload to SLP
SLP status message and		Factory Trim On site Trim
progress bar	Ready	
	Model (2 bytes) – configure by Cu Version (2 bytes) – configure by C Checksum (2 bytes) – generate automatic	ustom Info file ustom Info file cally from Program file

4 Download to Device

The SLP is able to download data to up to 10 devices simultaneously. The target device(s) should be connected to SLP either via the 10 pieces 3P Header or the 40P Box Header. Please refer to the product's user guide for SLP setup details.

4.1 Downloading Time

The following table listed the downloading time from SLP to various DC6688 and DC6388 products:

			Downloading Time			
Target	Device	Flash Size	4MHz	12MHz	Built-in OSC	
			Resonator	Resonator	@12MHz	
	F2SCN	2KB	1.6s	1.4s	-	
	F2STR	2KB	-	-	1.6s	
	FSE	30KB	-	4.2s	-	
		62KB	-	8.2s	-	
	FST	30KB	-	-	4.5s	
DC6688	FLE	32KB	-	4.6s	-	
		32KB	-	-	4.8s	
	FLT	64KB	-	-	8.4s	
		96KB	-	-	11.5s	
	DT	32KB	-	-	4.8s	
		96KB	-	-	11.5s	

4.2 40P Box Header

The main purpose of this interface is for programming setup in production. For further setup recommendation, please refer to the application note AppNote101 or contact Dragonchip technical support team.



Remarks:

J27 is newly added in SLP Rev3.2 J26 and J12 are fully compatible to those in SLP Rev3.1

	Pin	Name	Connection	Pin	Name	Connection
	1	LCD_P9	LCD module pin 9 (DB2)	2	GND	GND
	3	LCD_P8	LCD module pin 8 (DB1)	4	LCD_P10	LCD module pin 10 (DB3)
	5	LCD_P7	LCD module pin 7 (DB0)	6	LCD_P11	LCD module pin 11 (DB4)
	7	LCD_P6	LCD module pin 6 (E)	8	LCD_P12	LCD module pin 12 (DB5)
nt	9	LCD_P5	LCD module pin 5 (R/W)	10	LCD_P13	LCD module pin 13 (DB6)
le	11	LCD_P4	LCD module pin 4 (RS)	12	LCD_P14	LCD module pin 14 (DB7)
L	13	LCD_P3	LCD module pin 3 (VEE)	14	LCD_P15	LCD module pin 15 (LED+)
gn	15	LCD_P2	LCD module pin 2 (VCC)	16	LCD_P16	LCD module pin 16 (LED-)
Sİ.	17	LCD_P1	LCD module pin 1 (VSS)	18	GND	GND
S	19	GND	GND	20	NC	NC
A	21	CLK1	D1 XIN/ ECLK pin	22	GND	GND
in	23	CLK2	D2 XIN/ ECLK pin	24	GND	GND
Ω.	25	CLK3	D3 XIN/ ECLK pin	26	GND	GND
26	27	CLK4	D4 XIN/ ECLK pin	28	GND	GND
J2	29	CLK5	D5 XIN/ ECLK pin	30	GND	GND
	31	CLK6	D6 XIN/ ECLK pin	32	GND	GND
	33	CLK7	D7 XIN/ ECLK pin	34	GND	GND
	35	CLK8	D8 XIN/ ECLK pin	36	GND	GND
	37	CLK9	D9 XIN/ ECLK pin	38	GND	GND
	30	CLK10	D10 XIN/ ECLK pip	40	GND	GND

	Pin	Name	Connection	Pin	Name	Connection	
	1	LED_R_1	Red LED cathode for D1	2	GND	GND	
	3	LED_G_1	Green LED cathode for D1	4	LED_G_6	Green LED cathode for D6	
	5	LED_R_2	Red LED cathode for D2	6	LED_R_7	Red LED cathode for D7	
	7	LED_G_2	Green LED cathode for D2	8	LED_G_7	Green LED cathode for D7	
<u> </u>	9	LED_R_3	Red LED cathode for D3	10	LED_R_8	Red LED cathode for D8	
5	11	LED_G_3	Green LED cathode for D3	12	LED_G_8	Green LED cathode for D8	
Ĕ	13	LED_R_4	Red LED cathode for D4	14	LED_R_9	Red LED cathode for D9	
Ľ	15	LED_G_4	Green LED cathode for D4	16	LED_G_9	Green LED cathode for D9	
<u>0</u> .	17	LED_R_5	Red LED cathode for D5	18	LED_R_10	Red LED cathode for D10	
SS	19	GND	GND	20	NC	NC	
Ä	21	LED_G_5	Green LED cathode for D5	22	GND	GND	
⊆ ⊂	23	LED_R_6	Red LED cathode for D6	24	GND	GND	
ä	25	NC	NC	26	GND	GND	
12	27	KEY_CS	CHECKSUM Key (short to GND)	28	LED_G_10	Red LED cathode for D10	
	29	VCC_LED	Power supply for LED	30	GND	GND	
	31	VCC_LED	Power supply for LED	32	KEY_VF	VERIFY Key (short to GND)	
	33	VCC_LED	Power supply for LED	34	KEY_AUTO	AUTO Key (short to GND)	
	35	VCC_LED	Power supply for LED	36	NC	NC	
	37	VCC_LED	Power supply for LED	38	NC	NC	
	39	NC	NC	40	GND	GND	

	Pin	Name	Connection	Pin	Name	Connection
	1	NC	NC	2	GND	GND
	3	NC	NC	4	NC	NC
	5	NC	NC	6	NC	NC
	7	NC	NC	8	NC	NC
nt	9	NC	NC	10	VDD	Power supply for IC
e	11	NC	NC	12	VDD	Power supply for IC
μ	13	NC	NC	14	VDD	Power supply for IC
gn	15	PROG_A	PROG of D1-D5	16	VDD	Power supply for IC
Sić	17	PROG_B	PROG of D6-D10	18	GND	GND
AS.	19	GND	GND	20	NC	NC
A	21	ISPSEL/SL1	D1 ISPSEL/ SL	22	GND	GND
27 Pin	23	ISPSEL/SL2	D2 ISPSEL/ SL	24	GND	GND
	25	ISPSEL/SL3	D3 ISPSEL/ SL	26	GND	GND
	27	ISPSEL/SL4	D4 ISPSEL/ SL	28	GND	GND
J2	29	ISPSEL/SL5	D5 ISPSEL/ SL	30	GND	GND
	31	ISPSEL/SL6	D6 ISPSEL/ SL	32	GND	GND
	33	ISPSEL/SL7	D7 ISPSEL/ SL	34	GND	GND
	35	ISPSEL/SL8	D8 ISPSEL/ SL	36	GND	GND
	37	ISPSEL/SL9	D9 ISPSEL/ SL	38	GND	GND
	39	ISPSEL/SL10	D10 ISPSEL/ SL	40	GND	GND

5 Usage Consideration

5.1 Guidelines

- Ensure IC's VDD have a bulk capacitance of >10uF (more if additional load).
- Ensure IC's VDD rise time is <10ms.
- VDD, GND and SL cables connecting ICs to programmer should be twisted or shielded to minimize electromagnetic interference to the cable.
- If CLK signal is used, the cable should be twisted with GND or shielded individually to rest of the connection cables to minimize electromagnetic interference.
 - Power and signal relay should be added when cable length of >2m is required.
 - A resistor of 2~10ohms in series on VDD to each IC is recommended when using burn-in socket to program more than 5 ICs at a time.
 - Use the highest clock frequency available for programming if possible when burn-in sockets are used, ie not in-system program, for mass production. The clock source must be accurate (< ±0.5%) or alternatively use programmer's CLK output for programming.
 - Earth the GND and programmer case with a resistor of 1~10 Mega ohms in series, or use a reliable power adapter that earth the negative output for prolong (>1hr) programming operations to avoid buildup of static electricity.
 - Power adapter supplied by Dragonchip is rate as Office Equipment Use Only, it is not suitable for extensive operation period (>9 hours/day) or operation in non-office environment (Indoor, air-conditioned, safety and surge protected power mains). Therefore, it is required to source a suitable power adapter when the programmer is used outside the office conditions.

5.2 Gang Socket Board Usage Example

Here is usage example of a DC6688SLP-F2-X10 Rev2.0 gang socket board modified for mass production.



- Cable The VDD, GND and SL cable are twisted together to avoid electromagnetic interference (EMI). Shielding is unnecessary since the cable is only 15 cm in length. One should consider cable shielding if the cable length is >30cm and/or experience heavy EMI.
- Earth An earth terminal is created with 2 x 2Mega ohm resistors connected between the socket board GND plane and the terminal. Do not connect to this Earth terminal if the programmer or the power adapter has already earthed.



 VDD Resistor - A 10 ohm resistor is added to each burn-in socket VDD in series (Original VDD connection is cut and replaced by the red wiring connecting the cable connection port and the VDD resistor)

6 ESD damage prevention enhancement

Since the new built-in oscillator MCU series recommended using in-system programming for mass production, the risk of ESD damage from electrostatic charge built up on the PCBA has also been increase. Therefore as a precautionary measure, an ESD damage prevention circuit, is added to the enhanced SLP rev3.2 programmer (marked with round blue sticker, see photo below) to reduce the risk of ESD damage during the in-system programming process.

The damage prevention circuit dissipates any built-up of electrostatic charge on the PCBA when the PCBA makes contact with the programmer via the VDD and VSS lines, which are shorted to the Earth connection when the SLP is idle. This not only reduce the risk of damage to the programming IOs on the MCU during the in-system programming process, but also reduce the risk of ESD damage in the rest of the production process by removing electrostatic charge on the MCU.



Hardware with ESD prevention enhancement

'Software SLP Rev6.9.3' or higher is required to work properly.

Earth must be __ connected for ESD protection



It is important to note that this is only a precautionary measure and could not replace any ESD management that should be present in PCBA production line.

The following Earth check must be applied to make sure ground connection to the Earth (Power Ground) as little resistance as possible.

Earth Check (Important!)

Check **periodically** the resistance between the ground and Earth (R) < 20Ω . Otherwise, ESD discharge fails.



DragonFLASH[™]

7 Revision History

Document	Issued Date	Section	Page	Description	Edited by	Reviewed by
Rev No.						
1.0	Jun, 2015			First release for SLP Rev3.2	Celia Ki	Danny Ho
1.1	Jun, 2015			Updated section 3 J27 pin assignment	Danny Ho	Celia Ki
1.2	Sep,2015	5		SLP setup, Usage Consideration	Patrick Li	Danny Ho
1.3	May, 2016	4.2		Revise description on pin PROG	Danny Ho	Patrick Li
1.4	Oct, 2016	6		ESD section added	Danny Ho	Patrick Li
1.5	Dec, 2016	6		Add working instruction	Danny Ho	Patrick Li
1.6	Feb, 2017	6		Revise description	Danny Ho	Patrick Li
1.7	Mar, 2018	3.1		Update software SLP revision	Danny Ho	Patrick Li
		4.1		Added description for 6688BT		
1.8	Aug, 2018	6		Update description	Danny Ho	Patrick Li

The following table shows the revision history for this document.

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